Bi-weekly Status Report 2
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:

Over the course of the last two weeks, we did the following: gave our PIRM presentation; completed one teaching lab; began drafting two labs and a conceptual design of one additional lab; ordered PCBs for the data conversion evaluation module; completed the bill of materials for the evaluation module; and began high speed input anti-aliasing filter design. We also performed debugging of the firmware-to-software communication interface, and started porting the firmware to use FreeRTOS.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 11; Cumulative: 23)**
  - Completed PIRM presentation 1
  - Created preliminary RTOS architecture diagram
  - Began porting UART communications to an RTOS task
- **Sam Burnett (Bi-weekly: 18, Cumulative: 101)**
  - Ordered PCBs for data conversion evaluation module
  - Completed bill of materials for evaluation module
  - Simulated frequency response of input passband
  - Researched anti-aliasing filter design options
- **Mitchell Hoppe (Weekly: 12; Cumulative: 86.0)**
  - Completed PIRM presentation
  - Updated the website to improve the design of the Documents, Reports page
  - Worked on the front-end to improve the usability
- **Max Kiley (Biweekly: 10; Cumulative: 101)**
  - Completed PIRM presentation 1.
  - Researched how to implement a RLC simulation for the lab
  - Began mocking ideas for a spring-mass-damper lab experiment for lab 1
  - Began simulating RLC responses for lab 1.
- **Emily LaGrant (Biweekly: 12; Cumulative: 91)**
  - Completed PIRM presentation 1
  - Completed draft of heart rate project lab
  - Put draft into LaTeX
  - Began peer reviewing heart rate lab
- **Isaac Rex (Bi-Weekly: 16; Cumulative: 155.5)**
  - Finished prototype of Controls Lab 1 circuit
  - Validated concept and obtained preliminary test data

    - Began writing Controls Lab 1
    - Prototyped Labview script for obtaining loop response

Pending Issues:

- Vivado not working to spec
- Control loop too stable, need to incorporate in to lab
- ~~Anti-aliasing~~ filter design is hard ☹

Plans:

- Isaac:
    - Build up simulation in SIMULINK
    - Adapt Labview script to work with DAD
    - Continue writing lab document
- Emily:
    - Peer review heart rate lab
    - Begin rough draft of photo restoration lab
    - Finish testing heart rate lab
- Brady:
    - Determine if mutexes will serve as a proper read-write resource lock
    - Review communication standard and consider possible improvements
    - Test Sam's PWM intuition lab with prototype PMOD
- Sam:
    - Build evaluation module for data converters
    - Test I/O signal chain for evaluation module
    - Validate SPI block functionality with evaluation module
    - Design anti-aliasing filter for high speed input
- Max
    - Continue planning restructure of lab 1 and 2 for EE 324.
    - Start creating a prototype of the mass-spring-damper-system
- Mitch
    - Continue work on integrating the Matlab GUI with the existing python code
    - Continue to improve the design of the website.